Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**ANODE**

**.035”**

**.035”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004” min.**

**Backside Potential: CATHODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .035” X .035” DATE: 11/4/21**

**MFG: MOTOROLA THICKNESS .008” P/N: MZC4.75A5**

**DG 10.1.2**

#### Rev B, 7/1